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Re Applic of	Darren L. Anand et al.
Docket No.	FIS920010253US1
Serial No.	10/026,118
Filing Date	December 21, 2001
Attorney	Steven Capella

**FAX RECEIVED**

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Attached: Amendment; non-final

TECHNOLOGY CENTER 2800

Petition for Extension of Time Under 37 CFR 1.136a

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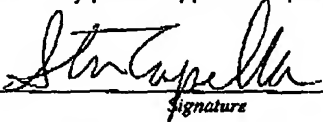

EXAMINER: Ly D. Pham  
ART UNIT: 2818  
FAX NO: 703-872-9318  
PHONE NO: 703-872-9317

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**INTERNATIONAL BUSINESS  
MACHINES CORPORATION**

Intellectual Property Law  
East Fishkill Facility  
2070 Route 52  
Hopewell Junction  
New York 12533-6531

Fax: 845-892-6363  
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<b>AMENDMENT TRANSMITTAL LETTER (Large Entity)</b>				Docket No. <b>FIS920010253US1</b>	
Applicant(s): <b>Darren L. Anand et al.</b>					
Serial No. <b>10/026,118</b>	Filing Date <b>December 21, 2001</b>	Examiner <b>Ly D. Pham</b>	Group Art Unit <b>2818</b>		
Invention: <b>FLEXIBLE MULTIBANKING INTERFACE FOR EMBEDDED MEMORY APPLICATIONS</b>					
<u><b>TO THE ASSISTANT COMMISSIONER FOR PATENTS:</b></u>					
Transmitted herewith is an amendment in the above-identified application. The fee has been calculated and is transmitted as shown below.					
<b>CLAIMS AS AMENDED</b>					
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST # PREV. PAID FOR	NUMBER EXTRA CLAIMS PRESENT	RATE	ADDITIONAL FEE
TOTAL CLAIMS	16	20	0 x	\$18.00	\$0.00
INDEP. CLAIMS	2	3	0 x	\$84.00	\$0.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					\$0.00
<b>TOTAL ADDITIONAL FEE FOR THIS AMENDMENT</b>					<b>\$0.00</b>
<div style="display: flex; justify-content: space-between;"><div><input checked="" type="checkbox"/> No additional fee is required for amendment. <input type="checkbox"/> Please charge Deposit Account No. _____ in the amount of _____ A duplicate copy of this sheet is enclosed. <input type="checkbox"/> A check in the amount of _____ to cover the filing fee is enclosed. <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. <b>09-0458</b> A duplicate copy of this sheet is enclosed. <input checked="" type="checkbox"/> Any additional filing fees required under 37 C.F.R. 1.16. <input checked="" type="checkbox"/> Any patent application processing fees under 37 CFR 1.17.</div><div style="text-align: right;"><b>FAX RECEIVED</b> <b>FEB 03 2003</b> <b>TECHNOLOGY CENTER 2800</b></div></div> <div style="display: flex; justify-content: space-between; margin-top: 20px;"><div> _____ <i>Signature</i> <b>Steven Capella, Registration No. 33,086</b> <b>International Business Machines Corporation</b> <b>2070 Route 52</b> <b>Hopewell Junction, New York 12533</b> <b>845-894-3669</b></div><div><b>Dated: February 3, 2003</b></div></div>					
<div style="display: flex; justify-content: space-between;"><div>CC:</div><div style="border: 1px solid black; padding: 5px; width: 300px;"><div style="font-size: small;">I certify that this document and fee is being faxing on February 3, 2003 and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.</div><div style="text-align: center; margin-top: 10px;"> <i>Signature of Person Faxing Correspondence</i></div><div style="text-align: center; margin-top: 5px;"><b>Colleen J. Dew</b> <i>Typed or Printed Name of Person Faxing Correspondence</i></div></div></div>					

I hereby certify that this correspondence is being deposited by FACSIMILE to the Commissioner of Patents and Trademarks, Washington, DC on February 3, 2003 by Colleen Dew.

Colleen J. Dew

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit 2818

In re application of \_\_\_\_\_ : February 3, 2003  
Darren L. Anand et al. : Examiner: Ly D. Pham  
Serial No. : 10/026,118 :  
Filed: December 21, 2001 : IBM Corporation  
Title: FLEXIBLE MULTIBANKING : Dept. 18G/Bldg, 300-482  
INTERFACE FOR EMBEDDED : 2070 Route 52  
MEMORY APPLICATIONS : Hopewell Junction, NY  
12533-6531

Amendment

Commissioner for Patents and Trademarks  
Washington, D.C. 20231

Sir:

Kindly amend the claims as follows:

- 1 1. (amended) A multibank DRAM macro, said macro comprising:
- 2 (a) a plurality of DRAM memory banks, each bank respectively
- 3 comprising:
- 4 (i) an array of DRAM memory cells,
- 5 (ii) bitlines and wordlines, respectively defining columns and
- 6 rows of the array,
- 7 (iii) a dedicated row address decoder circuit,
- 8 (iv) a column address decoder circuit,
- 9 (v) dedicated spare rows and columns for redundancy,
- 10 (b) a dedicated bank select input for each respective bank, each bank
- 11 input controlling operation of its respective bank,
- 12 (c) a data path receiver / driver shared by at least two banks.